ANNAN XIONG

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EDUCATION

The Hong Kong University of Science and Technology — Hong Kong SAR
Ph.D. in Electronic and Computer Engineering — *Sept 2020 - Sept 2025*

- Affiliation: Emerging Device and System Group/AI Chip Center for Emerging Smart Systems (ACCESS)
- Advisor: Prof. Mansun Chan
- HKUST Postgraduate Studentship

University of Electronic Science and Technology of China — Chengdu, China
B.Sc. in Electronic Information Science and Technology — *Sept 2016 - June 2020*

- GPA: 3.87/4.0
- Outstanding Student Scholarship (2016 - 2017, 2017 - 2018, 2018 - 2019)

Technion – Israel Institute of Technology; University of California, Santa Barbara; Massachusetts Institute of Technology — USA / Israel
Summer School & Exchange Programs — *2018 – 2019*

- Completed multiple international academic programs, including a visiting scholarship at Technion with ML-focused research training; an exchange term at UCSB with a 4.0 major GPA; and the MIT–UESTC summer program involving frontier engineering workshops, where a team-lead role was undertaken.

ACADEMIC APPOINTMENTS

AI Chip Center for Emerging Smart Systems — Hong Kong SAR
Postdoctoral Fellow — *Nov 2025 - Present*

PROJECT EXPERIENCES

Adaptive Depth Processing System Design Based on Foundation Transformers and Time-of-Flight Fusion, ACCESS

· Developed an adaptive and complementary depth processing system that unifies Time-of-Flight (ToF) sensing and Monocular Depth Estimation (MDE) into a single monocular pipeline. The system addresses the intrinsic limitations of single-sensor depth estimation by mitigating ToF sensitivity to noise, reflection, and multi-path interference while also resolving the scale ambiguity of MDE. At the same time, it removes the alignment and calibration complexity associated with multi-sensor setups. By jointly exploiting active ToF signals and passive monocular depth cues, the architecture achieves robust, physically reliable, and scene-consistent depth estimation across diverse environments.

· Integrated the retained 8-bit DepthAnything v2 foundation transformer to provide high-quality, zero-shot monocular depth priors, enabling accurate depth estimation without task-specific retraining and ensuring strong cross-domain generalization.

· Proposed the ToF-MDE-ViT-Fusion (TMVF) method, combining MoM-based global alignment, dual incrementing filling, and spatial consistency refinement to generate metrically reliable and high-fidelity depth maps.

· Realized a hardware–algorithm co-design that deploys ISP pre-/post-processing on an MPSoC FPGA and accelerates DepthAnything v2 inference on a dedicated 28-nm ASIC, achieving 27.6 GOPS/frame throughput, 36.4 ms latency, and 1.9 W power consumption.

· Demonstrated strong zero-shot generalization on synthetic and real-world datasets (FLAT, TICaM, CB, and in-house ToF), achieving up to 43.8% MAE reduction and 26.0% SSIM improvement over ToF-only baselines.

· The decoupled sensor–model architecture enables plug-and-play ToF cameras and depth foundation models while maintaining strong scalability toward higher resolutions and larger models.

Hardware-Software Co-design for a Deep-Learning-Based Indirect ToF ISP, ACCESS

- Proposed, trained and quantized a 4/8-bit U-net model with 96.5% sparsity for processing the ToF multichannel raw data directly, which can reduce the ToF shot noise, Multipath Interference (MPI) and motion artifacts.
- Implemented and tested the model with Verilog HDL on a proposed deep-learning-based indirect ToF ISP based on the VCU118 FPGA with the convolution engine, upsample engine and data buffer with DDR.
- Evaluated the ISP on both the FLAT dataset and the Microsoft Kinect V2 camera with 9-channel raw input data. Experiment results show that the ISP can effectively reduce the shot noise, MPI and motion artifacts simultaneously with a speed of 85.9 ms and 5.8 cm MAE.
- Proposed an extended 8-bit ISP to reduce the motion artifacts while achieving the aforementioned functions.
- This work was further extended into a generic 2D/3D deep-learning-based ISP framework and also generalized into an 8-bit GAN-based virtual staining pipeline for cancer surgery, reusing the quantization, sparsity, and hardware-efficient design principles to enable low-latency biomedical image translation on a U250 FPGA.

Device and Circuit Design for Indirect ToF Sensor Chips, HKUST

- Designed and simulated different indirect ToF photonic demodulators with different doping structure and concentration, including pinned photodiode, photogate, gate-assisted photonic demodulator and junction-assisted photonic demodulator in Sentaurus TCAD.
- Designed and taped out the ToF testing chip based on the TSMC 180nm 1P6M process, including the schematic and layout for the pixel, CDS amplifiers, decoders, modulation clocks, drivers and pads in Cadence Virtuoso.
- Tested the ToF chip with dedicated FPGA and PCB testing platform including off-chip LDO, clock and ADC.
- Proposed a device named Gate-Assisted Photonic Demodulator with Contrast Enhancement (GAPD-CE). The fabricated device achieves an 83% Modulation Contrast (MC) at 1 MHz and a 57% MC at 30 MHz. The result demonstrated the GAPD-CE is potentially a good candidate for ToF products.

SELECTED PUBLICATIONS

1 **A. Xiong**, P. Dong, Y. Tan, Y. Jiao, X. Liu, M. Yung, A. Li, P. Luo, L. Liang, J. Yuan and M. Chan, "An Adaptive Depth Processing System Based on Foundation Transformers and Time-of-Flight Fusion," *IEEE Transactions on Circuits and Systems I: Regular Papers,* 2025 (Accepted).

2 **A. Xiong**, Y. Jiao, X. Liu, M. Yung, X. Hu, L. Liang, J. Yuan and M. Chan, "An End-to-End Deep-Learning-Based Indirect Time-of-Flight Image Signal Processor," *IEEE International Symposium on Circuits and Systems*, 2024.

3 **A. Xiong**, S. Dai, C. J. Estrada, Z. Peng, C. Xu, J.G. Yuan and M. Chan, "A CMOS-Compatible Gate-Assisted Photonic Demodulator With Contrast Enhancement for Time-of-Flight Sensing," *IEEE Journal of the Electron Devices Society*, 2023.

4 S. Dai, C. J. Estrada, **A. Xiong**, C. Xu, J. Yuan and M. Chan, "A CMOS-Compatible Photonic Demodulator With Low-Power Consumption for Time-of-Flight Image Sensor," *IEEE Transactions on Electron Devices*, 2022.

PROFESSIONAL SKILLS

- **Software:** Vitis, Vivado, Synopsys Design Vision, Synopsys VCS, Cadence Innovus, Cadence Xcelium, Modelsim, Cadence Virtuoso, Altium Designer, Sentaurus TCAD, Origin Pro
- **Programming Languages:** Python, Verilog HDL, Verilog-A, MATLAB, C++, LaTeX
- **Deep Learning Framework:** PyTorch, TensorFlow
- **Natural Languages:** Chinese (native), English (fluent)

STANDARD TESTS

TOEFL	104 (Reading:27 Listening:29 Speaking:23 Writing:25)
GRE	322 (Quantitative: 166 + Verbal: 156) + Analytical Writing: 3.5

SERVICES AND EXPERIENCES

Teaching Assistant

- ELEC 2400 (Electronic Circuits, Prof. Kevin J. Chen), Spring 2021, HKUST
- ELEC 1010 (Electronic and Information Technology, Prof. George J. Yuan), Fall 2021, HKUST
- EESM 6980M (MSc Project, Prof. Khawar Sarfraz and Prof. Mansun Chan), Fall 2022, HKUST
- EESM 6980M (MSc Project, Prof. Khawar Sarfraz and Prof. Mansun Chan), Spring 2023, HKUST

Student Activity

- President of UESTC English News Agency, 2017-2018, UESTC
- Student Affairs Assistant of School of Physics, 2019-2020, UESTC
- Chinese National Level 3 Tennis Referee: provided referee services for Sichuan Provincial Collegiate Tennis Games, UESTC Autumn Tennis Games.